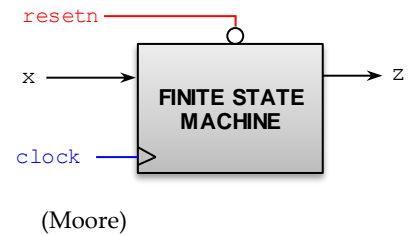# Solutions - Quiz 4

(April 6th @ 5:30 pm)

PROBLEM 1 (35 PTS)

- The following FSM has 4 states, one input x and one output z.
    - ✓ The excitation equations are given by:
        - $Q_1(t+1) \leftarrow Q_0(t)$
        - $Q_0(t+1) \leftarrow \bar{x} \oplus Q_1(t)$
    - ✓ The output equation is given by: $z = \bar{x} \oplus Q_1(t) \oplus Q_0(t)$

    - ✓ Provide the Excitation Table and the State Diagram (any representation).
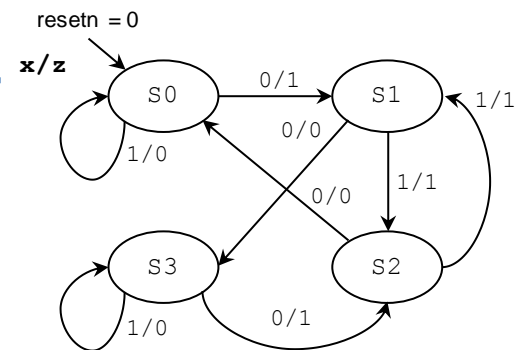   - ✓ Which type is this FSM? Circle or mark the correct one: (Mealy)   (Moore)

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State Assignment: S0: Q=00, S1: Q=01, S2: Q=10, S3: Q=11

x	Q_1Q_0 (t)	Q_1Q_0 (t+1)	z
	PRESENT STATE	**NEXTSTATE**	
0	0 0	0 1	1
0	0 1	1 1	0
0	1 0	0 0	0
0	1 1	1 0	1
1	0 0	0 0	0
1	0 1	1 0	1
1	1 0	0 1	1
1	1 1	1 1	0

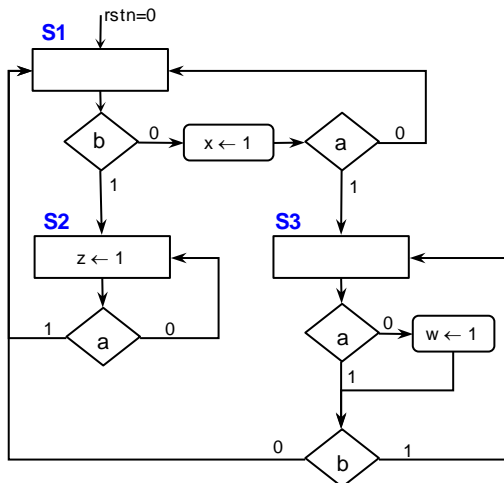| x	PRESENT STATE	NEXT STATE	z
0	S0	S1	1
0	S1	S3	0
0	S2	S0	0
0	S3	S2	1
1	S0	S0	0
1	S1	S2	1
1	S2	S1	1
1	S3	S3	0

PROBLEM 2 (35 PTS)

- Draw the state diagram (in ASM form) of the FSM whose VHDL description is listed below:

```
library ieee;
use ieee.std_logic_1164.all;

entity myfsm is
   port ( clk, rstn: in std_logic;
          a, b: in std_logic;
          x,w,z: out std_logic);
end myfsm;
```

✓ Circle or mark the correct FSM type:
(Mealy)   (Moore)

```
architecture behavioral of myfsm is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (rstn, clk, a, b)
  begin
     if rstn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
           when S1 =>
              if b = '1' then y <= S2;
              else if a = '1' then y <= S3; else y <= S1; end if;
              end if;

           when S2 =>
              if a = '1' then y <= S1; else y <= S2; end if;

           when S3 =>
              if b = '1' then y <= S3; else y <= S1; end if;
        end case;
     end if;
  end process;

  Outputs: process (y,a,b)
  begin
     x <= '0'; w <= '0'; z <= '0';
     case y is
        when S1 => if b = '0' then x <= '1'; end if;
        when S2 => z <= '1';
        when S3 => if a = '0' then w <= '1'; end if;
     end case;
  end process;
end behavioral;
```

PROBLEM 3 (30 PTS)

- Sequence detector: Draw the state diagram (any representation) of an FSM with input x and output z. The detector asserts $z = 1$ when the sequence 11010 is detected. Right after the sequence is detected, the circuit looks for a new sequence.

resetn=0

S0

0   x

1

S1

x   0

1

S2

1   x

0

S3

x   0

1

S4

1   x   0 $z \leftarrow 1$